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STUDY THE OPTICAL AND ELECTRICAL PROPERTIES OF (AU/PS/P-SI/AL) THIN FILM PREPARED BY THE THERMAL EVAPORATION TECHNIQUE

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SUMMARY

This paper explores the effect of different etching currents on the optical and electrical properties of Au/PS/p-Si/Al heterojunctions. PS layers were prepared in p-type silicon wafers by use of the electrochemical etching (ECE) technique, and then the metallization with gold (Au) was deposited through thermal evaporation. The etching currents were adjusted (0.2, 0.4, and 0.6 mA), and the obtained heterojunctions were analyzed in terms of current voltage (I-V), capacitance voltage (C-V), and reflectivity. The most important results included the fact that the etching current was increased, which essentially enhanced the detection efficiency to 93% at 0.6 mA, and the rectification ratio, which was indicative of improved diode-like behavior. Also, the capacitance was found to reduce with the increased etching current, which was also due to the enlargement of the depletion region in the PS layer. Optical findings revealed an increase in reflectivity with an increase in etching currents, with the growth in surface roughness and the enhancement of light scattering being the main reasons. This finding demonstrates the vital importance of etching current in the control of the electrical and optical properties of PS-based heterojunctions. The paper adds useful information to the optimization of porous silicon devices to be used in optoelectronic devices, showing how microstructural alterations can be used to influence performance. The future directions of the work should be further optimization of etching parameters, the effect of various objective electrolytes in their make-up, and the stability of such heterojunctions over time to be put into practical use as photodetectors, solar cells, and sensors, among others. Also, it will be important to scale up the fabrication process whilst ensuring high performance, as this will be essential in implementing the fabrication process in the real world.

Key words: *porous silicon, electrochemical etching, gold deposition, optical properties, electrical characteristics, heterojunction.*

INTRODUCTION

Porous silicon (PS) exhibits unique and tunable properties such as a direct and wide modulated energy band gap, high resistivity, and an extremely large surface area-to-volume ratio, while maintaining the same single-crystal structure as bulk silicon [1]. Metal–semiconductor junctions are fundamental in a wide range of microelectronic and optoelectronic devices. Silicon, specifically porous silicon, is especially suitable for such uses because of its exceptional electrical and optical properties, mechanical stability, and compatibility with standard silicon-based microelectronics, which has the added benefit that it is less expensive to fabricate [2][16]. The porous silicon structures are usually made by the electrochemical etching (ECE) of the crystalline silicon wafers with the solutions of hydrofluoric acid (HF) and organic solvents, including ethanol (C_2H^-OH) [3][18]. The PS layer that is obtained is typically sandwiched between the crystalline silicon [c-Si] substrate and a metal contact layer. The metal–semiconductor interface is a complex region whose physical and electrical properties depend strongly on surface preparation conditions. Interface states and chemical interactions between the metal and semiconductor at this junction significantly influence the electrical behavior and performance of the device [4].

Such interfaces with gold (Au) are promising to use due to its high electrical conductivity, chemical inertness, and great optical response in the visible spectral range [5][14]. To achieve the aim of transparency, flexibility, and low material and cost of electronic devices, the creation of ultra-thin gold layers (UTGLs) is receiving growing interest in recent years [6]. These thin films are typically prepared by physical deposition techniques, which include magnetron sputtering, thermal evaporation, chemical vapor deposition (CVD), and atomic layer deposition (ALD) [7].

Mechanism Metallic thin films, such as Au, grown on solid surfaces normally obey the Volmer-Weber mechanism, and occur in four different steps:

i. Nucleation and cluster formation,
ii. Diffusion-mediated coalescence,
iii. Adsorption-driven cluster growth, and
iv. Vertical grain growth [8].

These developmental processes are very important in determining the morphology, conductivity, and optical properties of the formed thin films.

Porous silicon (PS) is receiving much attention due to its specific characteristics, which include a modulated energy band gap, high resistivity, and a large ratio of surface area and volume, which is ideal in the application of microelectronic and optoelectronic devices. These devices heavily depend upon the nature of the metal-semiconductor junctions, and gold (Au) would be a perfect metal for such a junction, as gold is a conductive material with excellent semiconductor characteristics, chemical stability, and optical characteristics [20]. The electrochemical etching (ECE) process coupled with gold deposition is an affordable way of producing high-performance devices. This study examines the effects of the etching currents on the microstructure of the PS layer, its optical and electrical properties. Maximization of these properties can help produce more efficient optoelectronic devices, which are applied in solar cells, light-emitting diodes, and sensors, as well as improving silicon-based devices at a lower cost.

- The impacts of different etching currents on optical and electrical properties of the Au /PS /p-Si/Al heterojunction are explored in this paper to gain a better insight into the role of microstructural variations within porous silicon on device operation.
- It additionally brings out the effects of etching current on the reflectivity, capacitance, and current-voltage characteristics, providing useful information on the optimization of these properties in improved optoelectronic and photonic applications.
- The study contributes to the development of cost-effective fabrication techniques, using electrochemical etching and gold deposition, to improve the efficiency and performance of silicon-based microelectronic devices while reducing material costs.

The paper is presented in the following manner: Section 1 is the introduction of the importance of porous silicon (PS) and its use in microelectronics, particularly in metal-semiconductor junctions, and the need for using electrochemical etching to make high-performance devices. Section 2 describes the materials and methods used, i.e., the preparation of the substrate, the formation of porous silicon through electrochemical etching, the deposition of gold, and the characterization methods, i.e., I-V, C-V, and reflectivity measurements. Section 3 shows the result and discussion, which indicates the influences of the different etching currents on optical and electrical characteristics of Au/PS/p-Si/Al heterojunctions. Lastly, Section 4 provides the conclusion of this study summarizing the main findings, the importance of the results, and the further research directions recommended to make the fabrication process as efficient as possible and to investigate the possible applications.

LITERATURE SURVEY

In the recent research on porous silicon (PS), much attention has been given to how the technology can improve the performance of semiconductor devices since it can adjust electrical and optical characteristics [13][15]. Various studies have examined.

The effect of varying approaches to fabrication, including electrochemical etching, on the microstructure and surface morphology of PS layers [17]. These articles usually state that porosity and pore size distribution have a considerable influence on the reflectance and surface area that, in turn, affects the junction properties upon incorporation into the devices. Several other metal contacts on PS have also been studied by researchers in order to comprehend their contribution in transporting charges and creating barriers at the interface.

Over the past few years, academics have studied the behaviour of metal/PS/semiconductor heterojunctions with a particular focus on how deposition methods and post-processing manipulations can adjust electrical properties such as current voltage behaviour and capacitance [11]. According to these studies, the parameters of etching fabrication, such as etching current, etching time, and metal contact quality, are very important to minimize defects and enhance the movement of charge carriers. Another finding brought out by numerous experimental studies points to the fact that the addition of noble metals, e.g., gold, as contacts may lead to higher stability and lower losses due to recombination in PS-based devices [19]. A second line of current activity has examined the incorporation of PS into the real world of optoelectronics, e.g., in photodetectors and solar cells [12]. These studies prove the issue of enhanced light absorption that is attributed to the large surface area of porous structures and lower reflectivity. They also say that better sensitivity and shorter response times of the electrical response of PS heterojunctions can be customized. The study indicates that PS-based devices can be made to match traditional bulk silicon devices in some of the specialised applications with optimised structural parameters and interface quality.

In general, it is evident that the literature is moving towards a trend of establishing the role played by fabrication variables in the functional property of PS and heterojunctions. Nevertheless, further investigation of the impact of particular factors, such as etching current, on the essential performance parameters in the gold/porous silicon/silicon structures is necessary. This gap has inspired the current research, which tends to thoroughly examine these effects to give an understanding that can be exploited to build a more efficient design and manufacture of PS-based optoelectronic devices.

MATERIALS AND METHODS

The process of fabricating and characterizing the Au/PS/p-Si/Al heterojunctions is systematic in that it includes a series of substrates, creation of porous silicon layers, and deposition of gold, followed by a massive characterization of the film to measure the impact of different etching currents on optical and electrical characteristics of the completed device. This part provides the procedure that was used in the experiment.

Substrate Preparation

The second step involves the sequential immersion of P-type silicon wafers in methanol and ethanol to get rid of any surface contaminants. The wafers are rinsed in distilled water and dried using a stream of hot air, after which they can be processed further. To provide a good electrical contact, a thick layer of aluminum (Al) is deposited on the backside of the wafer by thermal evaporation.

Fabrication of Porous Silicon Layer

Creation of the porous silicon (PS) layer is done through the electrochemical etching (ECE) method. The silicon wafer, the p-type wafer, which has a resistivity of 2 Ω·cm, is dipped in an electrolyte solution of hydrofluoric acid (HF) and ethanol. Etching is done under controlled conditions, and the various etching currents (0.2, 0.4, and 0.6 mA) are used to carry out the etching process in a constant etching time of 25 minutes. These current differences during the etching process are employed to fine-tune the porosity and the morphology at the surface of the PS layer. The porous silicon layer is typified by having a large surface area, which improves its use in optoelectronics. Dividing the silicon wafers into 1.5 × 1.5 cm^2. Washing of p-type <100> Si wafers through a series of immersions in methanol and ethanol in order to decontaminate the surface. Washing with a lot of distilled water and drying in a stream of hot air. Beam etching of porous silicon in layers with the ECE process under controlled etching conditions. Both sides of the samples were made in ohmic contacts.

Gold Deposition

Once the process of etching has been done, the wafer is rinsed and dried. An aqua regia (Au) film is then deposited onto the porous silicon surface by the thermal evaporation process under vacuum conditions. Deposition is done under a vacuum of 10^{-6} Torr in order to achieve a consistent film thickness and the best attachment of the gold layer to the PS surface. The thickness of the gold film is the parameter that is regulated and tracked during deposition to achieve the same results with various samples. The thickness of the evaporated films on silicon substrates was determined gravimetrically using a Mettler AE-160 digital microbalance with a precision of 10^{-4} g. Current voltage (I-V) characteristics of the PS-Al junction were determined with the help of UNI-T UT61E digital multimeter and a LONG WEI DC PS-305D (30V) power supply [9].

Electrical Characterization

Standard current voltage (I-V) and capacitance voltage (C-V) tests are used to determine the electrical characteristics of the fabricated Au/PS/ p-Si /Al heterojunctions. The I-V characteristics are determined in the dark by applying a bias voltage and recording the current response. This analysis can be used to establish the rectifying action of the junction and the influence of etching currents of different magnitudes on carrier transport. The C-V characteristics are carried out to investigate the change in capacitance against the applied bias voltage, which gives information on the properties of the depletion region and how the morphology of the surface influences the behavior of the junction.

Optical Characterization

The optical characteristics of the Au/PS/ p-Si/Al heterojunction are determined by plotting the spectrum of reflectivity in the wavelength range (200-800nm). In this step, the optical response to the change of the etching currents of the PS layer in terms of the porosity and roughness of the surface will be investigated. The optical characterization aids in determining the interaction of the microstructural properties of the PS layer with incident light, which is essential for applications in photodetectors and solar cells in optoelectronics.

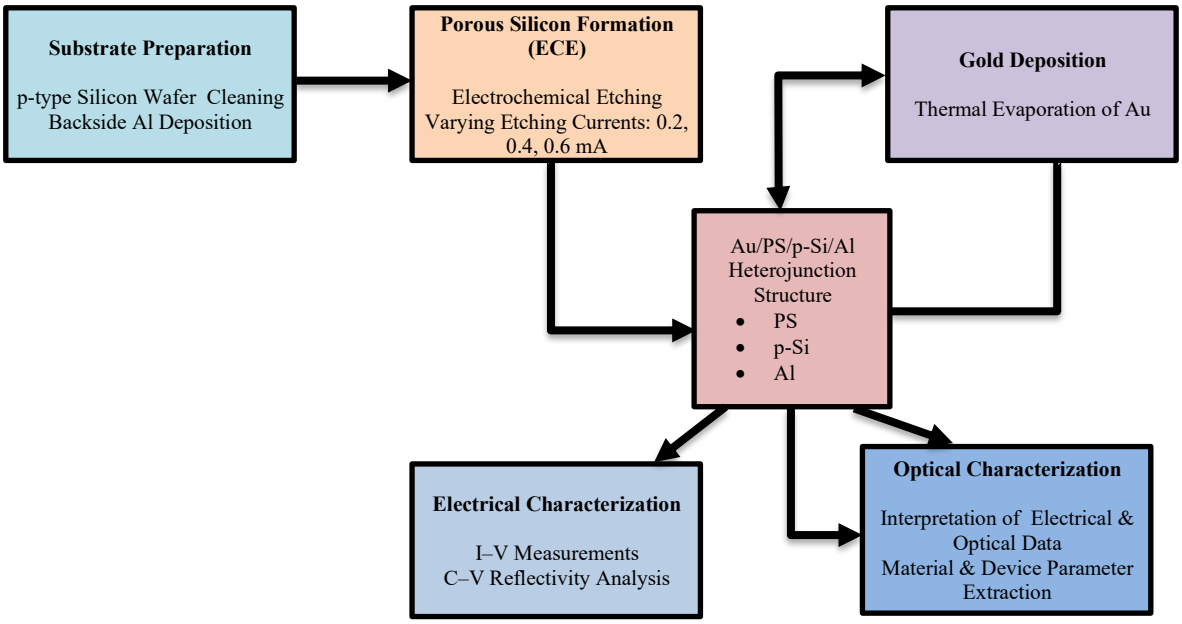

Figure 1. Fabrication and characterization process of Au/PS/p-Si/Al heterojunction

In figure 1 above shows the series of processes taken in the fabrication and characterization of the Au/PS/p-Si/Al heterojunction. It begins with the preparation of substrates, such as cleaning of the p-type silicon wafer and coating the backside with aluminum. Then, the porous silicon (PS) layer is created by using electrochemical etching (ECE) with different etching currents. After that, the PS layer is covered with a gold (Au) layer through thermal evaporation. The resulting heterojunction is then electrically and optically characterized through I-V and C- V measurements and reflectivity analysis, respectively, and used to evaluate material and device parameters and characterize the process. The figure gives a clear flow of the whole process, from fabrication to analysis.

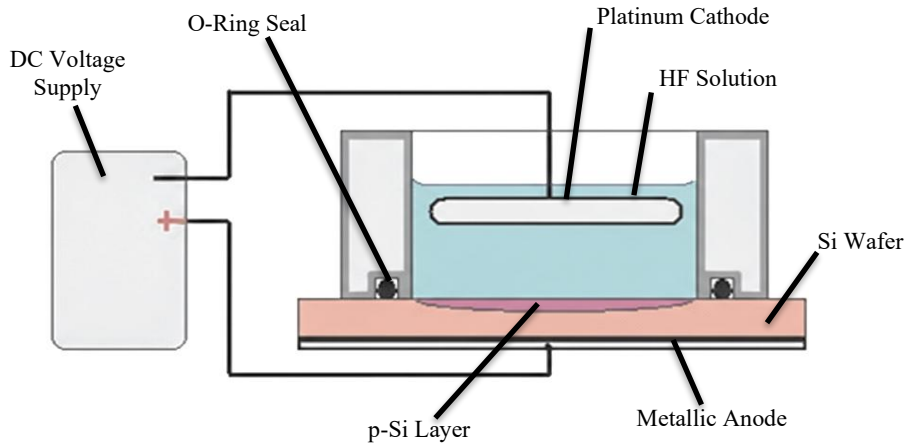

Figure 2. (a) Electrochemical circuit diagram; (b) cross–sectional view Au/PS/p-Si/Al sandwich structure

The circuit diagram of an electrochemical cell (Figure 2(a)) will show the experimental arrangement of the electrochemical etching process to be used to form a porous silicon (PS) layer. It depicts the p-type silicon wafer in hydrofluoric acid (HF) solution, a platinum cathode, and a metallic anode, so connected to a DC voltage supply. The positive terminal is used in connection with the anode, and the negative terminal with the cathode, which helps in the formation of the porous silicon layer. The final Au/PS/p-Si/Al heterojunction that is observed in the cross-sectional view figure 2(b) has the bottom coated with a thin layer of gold (Au) on top of the PS layer, then the p-type silicon (p-Si) and crystalline silicon (Crystalline-Si) layers are placed, and the bottom of the aperture is coated with a thick layer of aluminum (Al). This stratified architecture creates a sandwich architecture, which is part and parcel of the workings of the heterojunction.

The mathematical models used in the analysis of the Au/PS/p-Si/Al heterojunctions are based on the following equations:

Capacitance-Voltage (C-V) Relationship

The capacitance (C) of the junction can be related to the voltage (V) applied across the device using the following equation for a Schottky junction:

$$C(V) = \frac{1}{\sqrt{(V_{bi}-V)\cdot(V_{bi}+V)}} \qquad (1)$$

In equation (1), where V_{bi} is the internally supplied voltage, and V is the external bias voltage. The values of capacitance reduce with the increase in etching current because of the increase in the depletion region in the porous silicon layer.

Current-Voltage (I-V) Characteristics

The equation of the Schottky diode can be used to describe the I-V characteristics of the junction by equation (2)

$$I(V) = I_0\left(e^{\frac{qV}{kT}}-1\right) \qquad (2)$$

Where I_0 represents the saturation current, q is the charge of the electron, k is the Boltzmann constant, and T is the temperature. The equation models the rectifying behavior of the I-V characteristics of the Au/PS/p-Si/Al junction, with the current rising exponentially as the applied voltages rise.

Optical Reflectivity

The reflectivity of the interface between the Au/PS/p-Si could be written as a formula that is dependent on the wavelength (λ) and the refractive index of the materials to use. The roughness and porosity of the surface influence the reflectivity, and a modified Fresnel equation may be used to describe the reflectivity:

$$R(\lambda) = \left(\frac{n_1-n_2}{n_1+n_2}\right)^2 \qquad (3)$$

In equation (3), where $n_1$and n_2 are the refractive indices of porous silicon and air, respectively. The reflectivity spectra show the change in the surface properties and porosity of the PS layer under different etching currents.

RESULTS AND DISCUSSION

Optical Properties

The current density significantly affects the size, distribution, and morphology of the porous silicon nanocrystals, which in turn alter the optical response of the layer. In the short-wavelength region (ultraviolet to early visible range, approximately 200–500 nm), the reflectivity is relatively low. This behavior can be attributed to strong optical absorption caused by interband electronic transitions. In gold, such absorption is primarily due to transitions from the 5d band to the Fermi level (sp band), which markedly reduces reflectivity in this spectral region. At longer wavelengths (visible to near-infrared range, approximately 500–800 nm), the reflectivity increases because interband absorption diminishes, and the optical response becomes dominated by free conduction electrons oscillating under the influence of the incident electromagnetic field. Figure 3 illustrates the variation of reflectivity with wavelength for the Au/PS/p-Si structures fabricated under different etching currents. The results clearly indicate that the reflectivity behavior is strongly influenced by the etching current applied during porous layer formation.

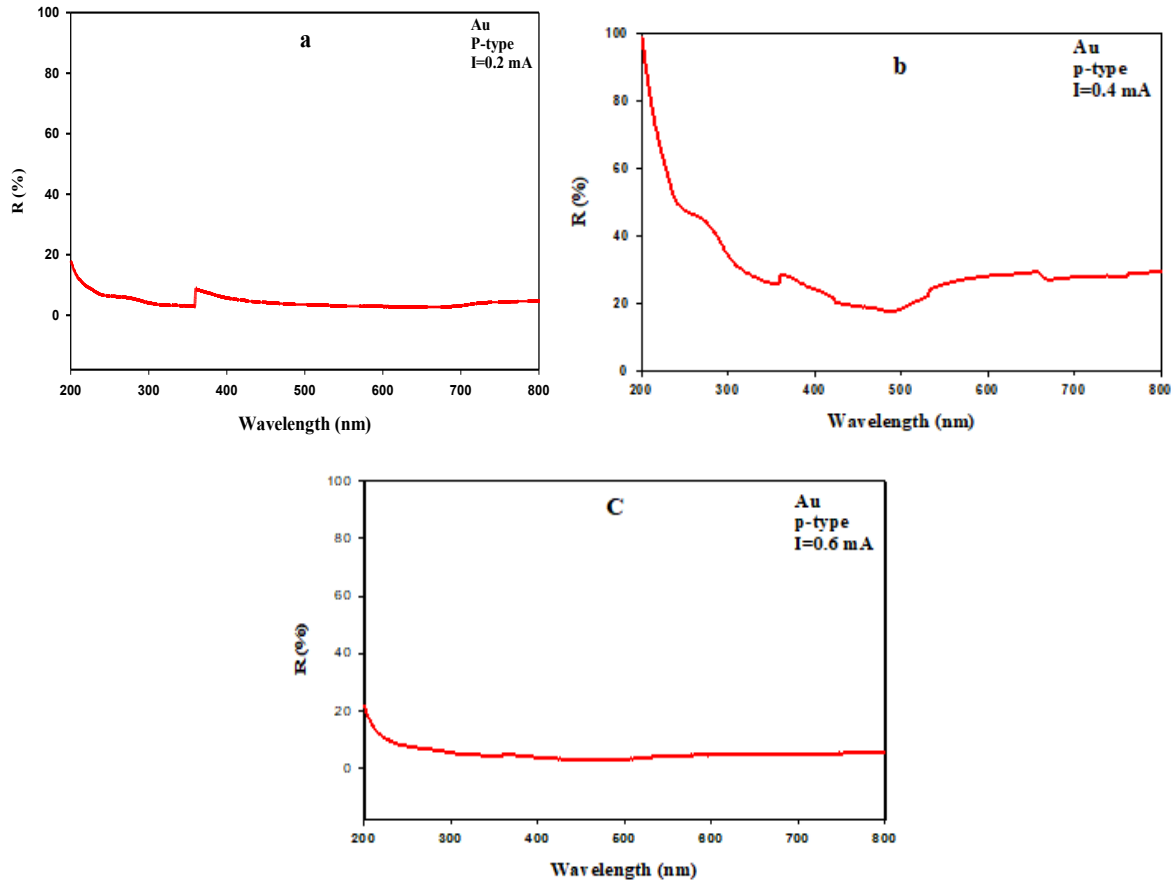

Figure 3. (a, b, c). Relationship between reflectivity (R%) and wavelength at different etching currents (I) (0.2 mA,0.4 mA, and 0.6 mA) at constant etching time, 25min

As illustrated in figure 3 (a, b, c), there is a significant change in the reflectivity spectra with an increase in etching current from 0.2 mA to 0.6 mA. This tendency implies that the increase of the current densities leads to the structural changes of the porous silicon layer, including changes in porosity, grain size, and surface roughness, which directly influence the optical characteristics of the deposited Au film. Increased surface roughness causes stronger light scattering in the interface, thus altering the effective reflectivity. Likewise, the crystallinity, as well as the density of the Au thin film, can vary and affect the electronic band structure of the metallic film, which may impact the absorption and reflection properties. In general, optical characteristics of gold-coated porous silicon layers are highly affected by

microstructural parameters, such as grain size, porosity, and film continuity, as well as the wavelength of incident light. Deposition conditions, such as etching current and evaporation rate, are thus categorical in customizing the optical output of Au/PS systems to be used in future applications in optoelectronic and photonic devices.

Capacitance–Voltage (C–V) Characteristics

In figure 4 presents the capacitance–voltage (C–V) characteristics of the Au/PS/p-Si/Al sandwich structure fabricated at different etching currents (0.2, 0.4, and 0.6 mA) while maintaining a constant etching time of 25 minutes. The C–V response of the structure is strongly influenced by the surface morphology and porosity of the etched silicon layer, which governs the effective dielectric properties and junction behavior. All three curves exhibit a similar general trend, yet the magnitude and rate of capacitance variation differ noticeably with increasing etching current.

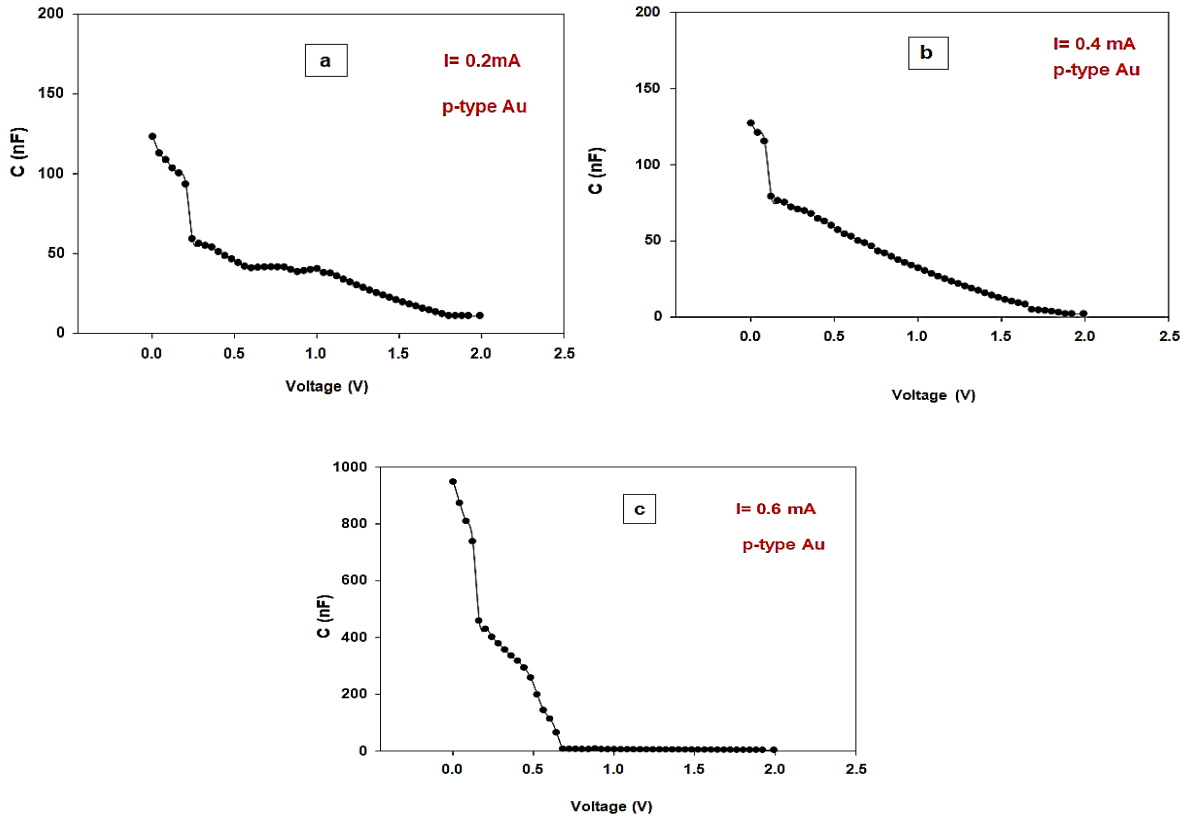

Figure 4 (a, b, c). The capacitance-voltage characteristics for different etching currents 0.2, 0.4 & 0.6 mA, at constant time 25min

In figure 4(a) illustrates that the sample that has been etched at 0.2 mA has a comparatively steep capacitance drop at a low applied voltage (approximately 0.15 V), but then a slow drop with an increase in the applied voltage. Figure 4(b) (0.4 mA) shows that the capacitance falls faster and takes lower values within a smaller range of voltages. In the case of the sample prepared at 0.6 mA (Figure 4(c)), capacitance reduces very sharply to almost zero at approximately 0.7 V, which means that junction characteristics have changed significantly. This progressive decrease of the capacitance with escalating etching current can be explained by the rise in the porosity and widening of the depletion layer in the porous silicon area. Very recently, it has been demonstrated that the more the etching current, the more porous and less conductive the resulting PS layer becomes, and therefore the longer is the depletion region and the lower is the overall capacitance of the junction. Besides, the expansion of the depletion region is associated with the augmentation of the built-in potential at the Au/PS interface. This response indicates the creation of a stronger Schottky-type junction with the raising of the etching current, which indicates the electric sensitivity of the structural properties of the porous layer.

Current–Voltage (I–V) Characteristics

This figure 5 shows the current-voltage (I-V) behavior of the Au/PS/p-Si/Al sandwich structures prepared with varying etching currents (0.2, 0.4, and 0.6 mA), having a constant etching time of 25 minutes. I–V measurements were done by sweeping through values of applied bias voltage of -5 V to +5 V and obtaining the corresponding current response. With the results, it is evident that the rectifying nature is present, which proves the existence of a heterojunction between the Au layer and the interface of porous silicon (PS). This correction has been attributed to the Schottky barrier developed at the metal-semiconductor interface that controls the movement of charge carriers across the interface.

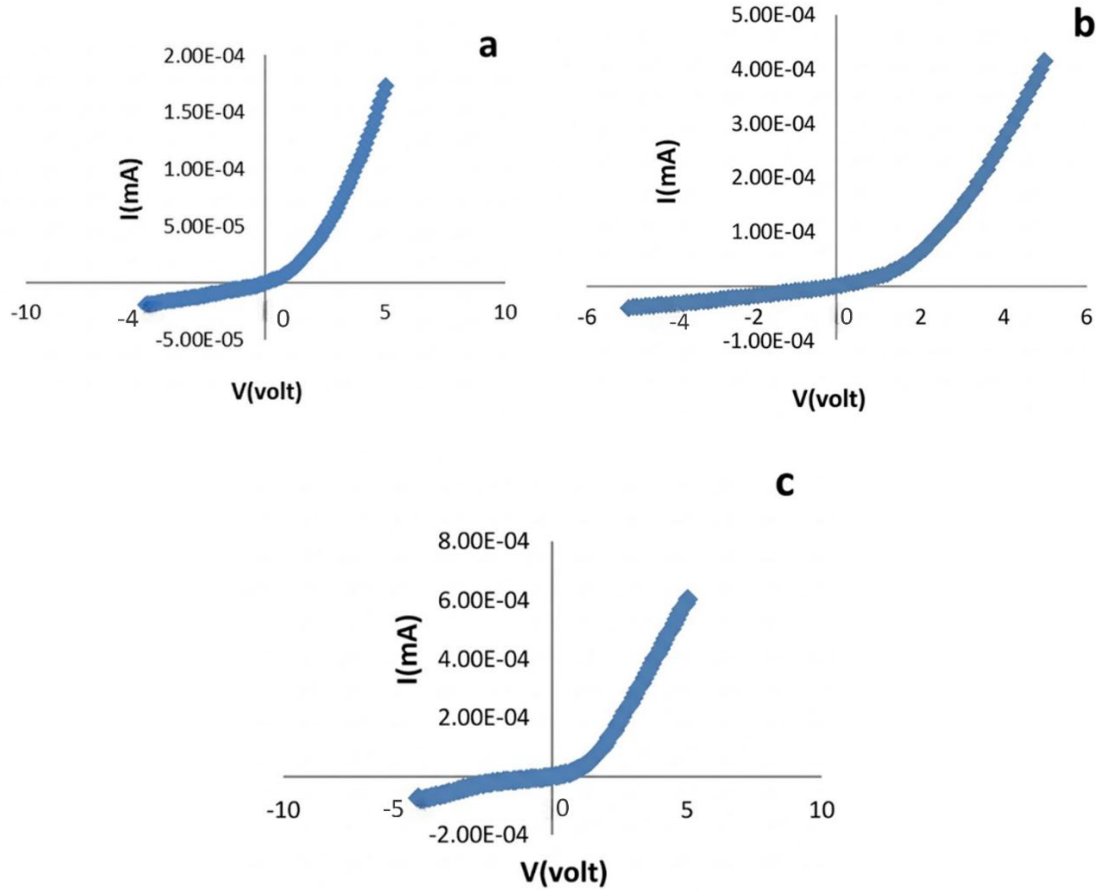

Figure 5 (a, b, c). Dark, forward bias, and reverse bias I –V characteristics of PS (a) 0.2, (b) 0.4, and (c) 0.6 mA at constant etching time 25 min

The figure 5(a) (sample etched at 0.2 mA) also shows that the current is very small at small values of the bias and rises non-linearly with the magnitude of applied voltage, showing typical diode-like products. In the case of the 0.4 mA sample (Figure 5(b)), the current also starts at low values but rises faster with voltage than in figure 4(a), indicating that there are now better conductivity and movement of carriers through the porous layer. With an increased etching current of 0.6 mA (Figure 5(c)), the current at zero bias is much larger, and there is a more linear or quasi-linear tendency in the I-V curve. The above behavior implies that the barrier height between the Au film and the porous silicon reduces at increased porosity, allowing easier movement of the charge carriers across the interface. The reason behind the observed positive change in forward current and negative change in the ratio of rectification could be due to the actual increase in density of the defect states and the increase in tunneling through the porous network. The existing conduction in such structures is majorly dictated by thermionic emission and diffusion of the minority carriers on the heterojunction interface [10]. I-V behavior variation with etching current is therefore the direct effect of microstructural variations in the pore size, porosity, and surface states on the electronic transport characteristics of the Au/PS/ p-Si/Al system.

CONCLUSIONS

This research paper has analyzed the effect of the different etching currents on the optical and electrical characteristics of Au/PS/p-Si/Al heterojunctions thoroughly, and the results were found to be very informative in terms of electrical and optical characterization. The findings revealed an improvement in some of the primary performance parameters of the etching and rectification ratio and the efficiency of detection as the etching current moved to higher levels of 0.6 mA. Higher etching currents gave a maximum possible detection efficiency of 93%, and a better rectification ratio was obtained, an indication of improved diode-like characteristics in the junction. The capacitance reduced as the etching current increased, and this can be explained by the fact that the depletion region was broadened and more porosity was formed in the silicon layer. This is in agreement with the structural adjustments that were witnessed in the porous silicon layer with an increase in etching current. Optical reflectivity measurements were also used to show that higher values of the etching current contributed to surface roughness and light scattering that enhanced the reflectivity, particularly in the visible to near-infrared range. The study provides valuable insights regarding the possibility of etching current to be used in improving the structural and functional properties of Au/PS/p-Si/Al heterojunctions as optoelectronics. These results indicate that etching current control is critical to optimizing the electrical and optical properties, and thus it is possible to optimize the performance of these devices and improve performance in photodetectors, solar cells, and sensors. The statistical analysis also brings out the fact that the optical and electrical properties, including the reduced capacitance and the enhanced reflectivity and rectification, are highly dependent on the etching current, and therefore, are another crucial parameter to use during the fabrication process. The further optimization of the etching settings, such as exploration of the various combinations of electrolytes, duration of etching, and temperature, should be the subject of future studies in this field in order to gain an insight into the combined impacts of these factors on the characteristics of the PS layer. Moreover, investigations into the long-term stability and performance of these heterojunctions under different conditions of the environment and operation would be of interest in the practical application of these heterojunctions. The increase in the scale of the fabrication process without lowering the performance of the devices and exploring the effects of various metal contacts on the junction characteristics will become a significant step towards commercial and industrial use of these devices. Also, the studies of the implementation of such heterojunctions into flexible, transparent, and inexpensive optoelectronic devices may provide a way to new opportunities in the sphere of wearable electronics, sensors, and low-cost devices.

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