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HIGH-PERFORMANCE ONE-STAGE BOOSTING PFC CONVERTERS WITH ADVANCED CONTROL FOR ENHANCED POWER QUALITY AND STABILITY

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SUMMARY

This article introduces an advanced controller technique, as well as a One-Stage Boosting Power Factor Correction (OSBPFC) converter. The proposed approach is oriented towards the creation of more powerful features (PQ), more desirable stability, and adherence to fundamental principles for input interfaces. This technique, which distinguishes it from typical strategies, provides a terrific dynamic response; it is evident that the upward propellant times are brief and the overshoot is minimal. It effectively avoids the drawbacks of conventional AC-DC converters and delivers better overall performance across a wide range of operating conditions. The performance ideal of the converter is investigated in MATLAB/Simulink modelling and compared with available alternatives. The constant-state behaviour of an 850 W converter under closed-loop control is analysed in some detail across a series of loading conditions. It delivers voltages that dictate the duration the converter can withstand unexpected load changes and delivery voltage faults. It has shown transient performance and power efficiency in a small device, with close-to-unity power factors and source current Total Harmonic Distortion (THD) of 1.17%. In addition, the proposed topology offers an impressive 97% operational efficiency. This type of investigation and advancement of strength conversion technologies, in most instances, forms the foundation for the development of strong controls that are assured to ensure proper policy and enhanced electrical properties.

Key words: *one-stage boosting power factor correction (OSBPFC), proportional integral method (PIM), power quality (PQ), MATLAB/simulink modelling, total harmonic distortions (THD), operational efficiencies.*

INTRODUCTION

The systems of power converters are inherent to the greening of the work of advanced electrical and electronic devices. These constructions are credited with transforming electrical power into other forms without consuming much energy. However, traditional converters face recurring challenges, such as low-power components, voltage regulation issues, and high harmonic distortion, especially under

various lower-than-load and supply scenarios. New custom methods and manipulation techniques are being developed and implemented to overcome these challenges as the impact of immortal appetite and the need for reliable, ecologically friendly energy conversion grow. Among these, more advanced control strategies, including the Proportional Integral Method (PIM), have been shown to have a promising impact on dynamic performance, stability, and fundamental efficiency. These strategies enable a more effective and efficient power conversion solution in many applications by quantifying the response, reducing overshoot, and minimising harmonic distortion. This paper explains why these improvements are necessary and how they are used to optimise structures in energy conversion, thereby improving overall performance in an advanced energy conversion system. Conventional Power Factor Correction (PFC) converters face significant constraints, including low conversion efficiency, poor dynamic response, and an inability to achieve low Total Harmonic Distortion (THD) when the load varies or the supply conditions change. Their reliance on multi-stage architectures adds components and complexity to the control system, increasing costs and reducing reliability. In addition, the lack of an adaptive control strategy limits their response and stability to observed rapid changes in loads. These issues are directly addressed by the proposed One-Stage Boosting PFC (OSBPFC) converter. This integrated control architecture relies on the Proportional Integral Method (PIM) to enable faster transient response, reduced overshoot, and improved power quality through minimised THD.

Recently, Power Factor Correction (PFC) conversions between modern and direct contemporary (AC-DC) applications have been enhanced to be more effective and efficient, while alleviating harmonic distortion. Through feed-ahead control, increased degrees of PFC conversion, based on serial capacitors, can amplify the input voltage and equalise the available [1]. Bridge-kind single-energy-conversion PFCs have disadvantages, including significant component count, low efficiency, and substantial power loss, although they are less expensive than their counterparts [2]. Regarding the convenience and speed of strength, it can be observed that conventional AC/DC conversions typically utilise amplified-type structures. However, these systems are regulated, making it difficult to downsize while maintaining effectiveness at higher output voltages and lower shifting frequencies [3]. The separate single-phase PFC networks are one measure to resolve these problems, offering high effectiveness while minimising harmonic distortions without compromising IEC standards [4]. These systems incorporate dual-switch forward conversions and boosted PFC regularly. There are also new on-board charging systems that allow electric vehicles (EVs) to be rapidly recharged with consistent voltage and power. These are discontinuous Luo DC-DC conversions and bridgeless high-voltage modified SEPICs [5].

Embedded step-up LLC resonance conversions with PFC functionality have also been used to improve overall performance and eliminate the need for standard boost devices [6]. The bidirectional AC-DC conversion process, enabled by high-bandgap devices, offers compact, efficient solutions for charging storage devices in electric vehicles [7]. Bridgeless PFC converters have become increasingly attractive as an alternative in recent years because they can be configured with a normal power factor, a constant DC voltage, and reduced complications due to their streamlined topologies [8]. Two of the most significant consequences of reactive damping systems aimed at addressing high-frequency electromagnetic interference (EMI) are increased power delivery and IEC 61000 compliance. By mitigating the aberrations under special loading conditions, advanced harmonics abatement methods, such as variable harmonics conductivity controls (AHCC), represent an additional step toward increasing PFC conversions beyond [10]. The reversible switching of strength and the flexibility of the system have been demonstrated with the Twinifest Dream Livebridge (DAB) system, which is based on total PFC conversions that store and apply to reversible AC-DC packages realised by confined ZVS zones [11]. Also, the Luo PFC converters in continuous enter-output strength reduced the voltage tension. They made it easy to manage in discontinuous conduction mode (DCM) and were suggested for global supply-voltage applications [12].

Even more impressive is the effectiveness of a wirelessly recharging device based on T-type converters, which achieves 96% effectiveness while maintaining a minimal total harmonic distortion (THD) of 1.27% [13]. These advances demonstrate how PFC techniques have evolved to meet the growing demand for improved AC/DC systems, offering excellent performance, size, and efficiency.

Dynamical efficiency and voltage purity under varying loads and supply voltages are two situations in which traditional AC-DC conversions, including Power Factor Correction, are technologically inferior [16]. Problems with slow instantaneous response, severe overestimation, and poor adaptation to varying electrical conditions are widespread in conventional PFC converters. Optimising total harmonic distortion (THD) is also challenging because existing solutions struggle to maintain low THD levels across a wide range of operating conditions [17]. These methods aren't practicable for current high-performance applications due to their complex concepts, the large number of their components, and diminished performance under less-than-ideal conditions. These operations require the use of highly efficient and high-quality energy.

Traditional topologies in PF C converters cannot keep pace with the growing requirements of ultimate energy purity under various operational circumstances, better dynamic response capability and excellent effectiveness, no matter how far the PF C converter frequency technology has gained. Critical circuits cannot take advantage of these conversions due to a lack of a comprehensive controlling approach that combines exact oversight with low total harmonic distortion THD and good operating effectiveness in the event of fluctuating loads and inputs [18]. Furthermore, to address the area and pricing limitations, most available systems compromise on element dimensions, difficulty, and cost, which limit their scalability and practical application. These problems and the need to drive in spur-of-the-moment, unforeseeable environments necessitate a higher-technology conversion architecture [19].

According to the existing literature, power conversion systems face a significant gap: advanced control strategies, including the Proportional Integral Method (PIM), are applied alongside high-performance PFC converters to achieve both high-quality dynamic response and power quality. Although individual studies have been conducted on separate variables, such as transient response, THD reduction, or efficiency, little has been done on overall solutions that deliver the desired results across all these variables in a single converter design [20]. 3 In contrast, the super software of excessively executed blunted tragedies presents nearness conjunction power elements, low THD and fantastically dynamic performances under linear situations, and under international situations [21]. There are gaps in the existing literature that call for a modularly scalable system that does not compromise operational efficiency across various load profiles and in the presence of supply chain disturbances. This master plan aims to fill this gap by developing a new design of converters that use innovative control mechanisms to improve regulation, power quality, and robust operation across different operating conditions. This work presents a new idea in the era of strength conversion: the One-Stage Boosting Power Factor Correction (OSBPFC) converter. This sophisticated process uses the Proportional Integral Method (PIM). The main aim of this work is to add beautiful energy to the law and to offer a dynamic response in AC-DC converters [22]. The suggested converter removes the limitations of traditional methods, thereby achieving higher performance across a broad spectrum of operating conditions. Those are the principal contributions of this study,

1. An original One-Stage Boosting Power Factor Correction (OSBPFC) converter is presented in this study. It combines the complex Proportional Integral Method (PIM) with real-time policies and more robust electrical characteristics, thereby setting it apart from traditional AC-DC converter designs.
2. The converters suggested are taken to super dynamic performance characterised by minimal upward thrusts and negligible overshoots, critically overcoming the problems of traditional approaches that cannot cope with low reaction instants and extra overshoots with variable load and source voltage under certain conditions.
3. The converter performance is critically examined. The application of Matlab/Simulink modelling demonstrates improved robustness to sudden load and voltage disturbances. Overall performance is therefore guaranteed during the alternation of source voltages and cargo scenarios [23].
4. The research involves hardware verification, running an eight hundred and fifty W execution Movement showing high excellence brief performance with regards to energy, with contemplating closer-solidarity energy elements with undergoing at 117% total harmonics distortion (THD), thereby confirming the realistic Feasibility and dependability of the speak the truth be converter.

5. The proposed converter topology has a proposed and outstanding operational efficiency of ninety per cent, which broadly enhances the energy conversion efficiency compared to the current ones and overcomes the performance issues in the traditional designs [24].
6. The experiment is used as the primary reference in the study of the destiny of robust control methods, to provide a document to design an excessive-performance strength converter with better regulation, dynamic reaction and power fine-tuning in diverse programs at the present energy structures.

The discussion begins with Section 2: Enhanced System Topology, which results in an advanced design methodology and broader performance operations to maximise device performance and reliability. This is also accompanied by Section Three: Innovative Control Architectures with Comprehensive System Modelling in Figure 1, which introduces innovative control strategies enabled by solid system modelling that lead to greater operational accuracy. Subsequently, Section 4: Analytical Study of OSBPFC Converter Dynamics via Simulation presents a detailed analysis of the converter's dynamics under different conditions, using simulation tools to extract meaningful insights. Lastly, the paper concludes with Section 5: Conclusion, which summarises the findings, provides a fundamental understanding of the study, and defines the future direction of developments in the topic [25] (see Figure 2).

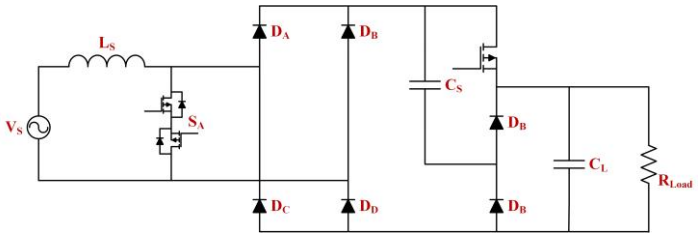
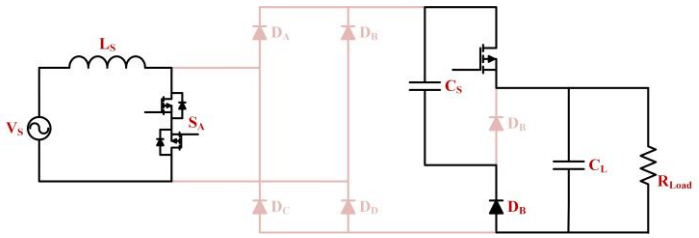
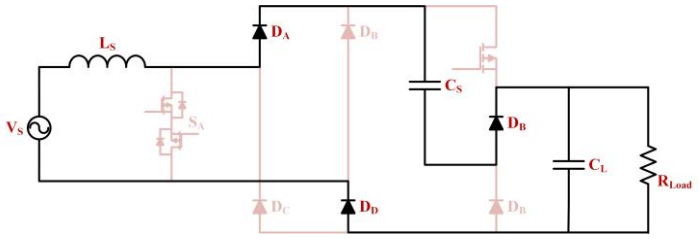


Figure 1. Architecture of the proposed SC-integrated power factor correction converter



(a)



(b)

Figure 2. Operational Modes of the Proposed Converter During the Positive Half-Cycle of AC Input: (a) When switches S and S1 are activated (b) When switches S and S1 are deactivated

REVIEW OF LITERATURE

Power factor correction (PFC) converters have advanced significantly as researchers strive to enhance efficiency, reduce harmonic distortion, and design compact single-stage converters for high-density modern power supplies. Conventional boost-type PFC converters exhibit high conduction losses, slow transient response, and complex control tuning, especially under varying loads or supply conditions [1], [2].

To help expand the balanced-current input-voltage operating range of series-capacitor-based PFC converters, Chen and Lan [1] proposed unequal-duty-ratio feed-forward control, but designing this model required several capacitive components, increasing the component count. A bridgeless totem-pole resonant single-power-conversion PFC converter proposed by Cho et al. [2] had lower conduction loss and a small circuit size. Still, the control synchronisation of the resonant network was more complex than that of the two-power-conversion converters.

Ghazali and Adib [4] invented a combined boost and dual-switch forward converter that provides soft switching. In their design, they were more efficient but were plagued with large magnetics and the extra gate-drive circuitry. Singh et al. [5] proposed a bridgeless modified high-step-up SEPIC PFC converter for charging light-EV batteries; it achieved a high step-up gain but lacked an extensive assessment of transient THD. Yue and Wang [6] removed the boost step by shaping an LLC resonant cell into a single-stage step-up converter, thereby enhancing the power factor. However, this required reasonable control of the resonant frequency to ensure stability.

Table 1. Reference table

S.no	Ref (Author, Year)	Topology / Mode	Control Method	Notable Performance Reported	Key Advantages	Limitations
1	[1]	Series-capacitor-based boost PFC (single-stage variant)	Unequal duty-ratio feedforward	Extends balanced-current input range; improved efficiency	Wider input range, improved current balancing	Increased control complexity; higher part count
2	[2]	Bridgeless totem-pole resonant single-stage PFC	Resonant switching control	High efficiency design targeting reduced switching loss	Low switching loss, compact architecture	Design complexity; timing sensitivity
3	[3]	High-frequency universal-input PFC	High-frequency PWM control	Operation at high frequency to reduce magnetics	Smaller magnetic components, universal input	EMI/noise issues at high frequency
4	[4]	Integrated boost + dual-switch forward (soft-switching)	Soft-switching control	Improved switching efficiency; higher power density	Reduced switching loss, high efficiency	More components; gate-drive complexity
5	[5]	Bridgeless modified high-step-up SEPIC for EV charger	PWM with bridging control	High step-up gain; efficiency validated for EV charging	Reduced conduction loss, suitable for EVs	Specialised for EV; limited generality
6	[6]	LLC-based single-stage step-up AC/DC (no boost stage)	Resonant LLC control	High PF for EV charging; integrated topology	Eliminates boost stage; high PF operation	Tuned for specific load/voltage range
7	[7]	Boost-inductorless, electrolytic-capacitorless bidirectional AC-DC	Bidirectional modulation control	Novel bidirectional operation with reduced volume	Compact, high-power density	Integration and control challenges
8	[8]	Bridgeless modified boost PFC for EV charging	Adaptive PWM / bridging	Improved PF and efficiency vs. bridged designs	Lower conduction losses	Light-load THD may increase without adaptation
9	[10]	Boost PFC with adaptive harmonic conductance control (AHCC)	AHCC adaptive harmonic control	Demonstrated THD reduction at light loads	Very low THD under light load	Complex harmonics estimator; tuning required
10	[11]	Semi-dual-active-bridge AC-DC with sinusoidal-ripple charging	Sinusoidal-ripple current modulation	Complete soft switching and PFC features	Reduced switching loss, soft switching	High component count; topology specific
11	[12]	Modified Luo PFC AC-DC (continuous I/O current)	PWM control for continuous I/O current	Works for universal supply voltage range (LVEV chargers)	Continuous I/O current, wide input range	High converter complexity; EV specific
12	[14]	Interleaved DCM boost PFC + LLC DC-DC (single-stage integration)	PI control + interleaving	Reduced bus voltage; good reported efficiency	Integrated design reduces stages and bus stress	Requires precise interleaving coordination

Zhang and colleagues [7] explored a bidirectional, inductance-free, capacitorless single-stage converter that can be used in compact EV chargers, minimising device size but placing greater stress on the device. Bridgeless modified boost topology with adaptive PWM in EV chargers was optimised by Dadhaniya et al. [8], which achieved power factors close to unity but at the cost of a low response speed at light loads. Zhu et al. [10] proposed an adaptive harmonic-conductance control that improved light-load THD in boost PFC converters. Still, the algorithm had to be tuned in a complex manner across different supply conditions.

To achieve a whole soft-switching operation, Hu et al. [11] applied sinuoidal-ripple-current charging modulation to a semi-dual-active-bridge AC2 DC converter, but with higher control overhead. Gupta and Singh [12] suggested a variation of the Luo PFC converter with continuous input-output current to supply voltage universal ranges, and stable operation was attained, but with complex control coordination. A T-type wireless-charging converter achieving 96% efficiency and 1.27% THD was investigated by Teeneti et al. [13], demonstrating that high-efficiency resonant topologies can be used in contactless power applications. Lu et al. [14] paired an interleaved DCM boost PFC with an LLC DC-DC stage, achieving lower bus voltage and excellent dynamic performance but requiring precise timing between interleaved legs.

In these works, researchers have tried to maximise switching loss, harmonic suppression, or transient response at the expense of the other two, usually none of the three together [5]-[14]. In addition, the majority of designs are based on multi-stage conversion or complex control laws, which increase cost, size, and scalability. Current analyses [16] -[19] reaffirm that the traditional PFC topologies continue to have difficulty sustaining low THD and rapid transient recovery across a wide range of loads, particularly when compactness and cost are of interest.

Table 1 summarises these findings and shows that most systems have efficiencies above 93% and THD below 3%, although only a small number have higher efficiencies and lower THD. The following observation constitutes a significant research gap: the need for a one-stage architecture that provides a near-unity power factor, extremely low THD, high dynamic stability, and simpler hardware. To fill this gap, this proposal is a One-Stage Boosting PFC (OSBPFC) converter that incorporates a high-performance Proportional-Integral Method (PIM) controller to improve dynamic response and power quality, with 97 per cent efficiency and 1.17 per cent THD under varying load conditions [22] -[24]. This high-quality upgrade provides a solid foundation for next-generation high-performance AC-DC power interfaces.

Enhanced System Topology: Design and Performance Operations

Figure 1 shows the suggested architecture. The circuit has a DC-link capacitance. C_L, a single reversible switch, four diodes D_A–D_D, two rapidly recovering diodes D_E and D_F, and a single-ended switch C_S. We built this architecture to work in CCM (constant-conductivity mode). The shifting losses are reduced because the voltages strain on switches. S_B It is half that of activated switches. S_A. There is no need for an additional voltage detector, as the PWM controls the voltage between Csw and Cdc.

Every alternating current half-cycle corresponds to one of 2 phases: Phase 1 and Phase 2. The functional circuitry for Phases 1 and 2 is shown in Figures 2(a) and 2 (b), respectively.

Phase 1: Turn on S_A and S_B. Here, inductance L_S receives its electricity from the incoming voltages, and V_{AB} Is equal to zero. The SC phase is complete when the loads draw power from the capacitor in synchrony. C_S and C_L, as shown in Figure 2(a). As demonstrated in Figure 3, the inductance is now being charged by passing V_S Over it.

Phase 2: Once you deactivate S_A and S_BThe machine will switch to Phase 2. Here, V_{AB}= $2V_L$, and the inductance charge C_S and C_L are transmitted via D_A and D_C, respectively, as shown in Figure 2(b). Figure 3 shows the voltages over the inductance, V_{Ls} = {V_S- (V_{CS}+V_L)}, in this scenario.

V_L is blocked by switching S_B, and $2V_L$ is blocked by switching S_A. Although it is similar to its operation during the positive half-cycle of an alternating current (AC), this section omits the converter's operation during the negative half-cycle. When the ac cycle is negative, D_B and D_D Take the position of D_A and D_C In terms of conductance in Figure 3.

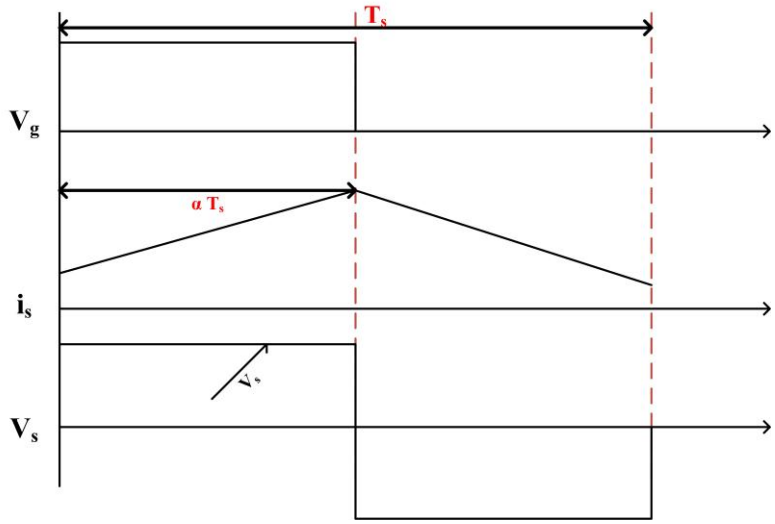


Figure 3. Output waveforms during steady-state conditions for the proposed converter

Expectations underlying the conversion evaluation are as follows.

1) Every part is perfect in every way.

2) The CCM governs the converter's operation.

3) During the shifting time, t_SAll capacitors are large enough to maintain a constant voltage.

4) Throughout t_SThe incoming voltages are relatively consistent.

The following is the expression for the input voltage and current, which are considered to have cyclic conduct:

$$V_S = \sqrt{2}v \sin \omega T \qquad (1)$$

$$I_S = \sqrt{2}i \sin \omega T \qquad (2)$$

Whereas the root-mean-square is the amplitude of the alternating flow voltages and electricity, respectively. ϋ represents the incoming rotational frequencies in rad/sec. Due to its sequential connection with the availability, the inductor's electricity (I_{LS}) is identical to the incoming electricity (I_S), and the voltages (V_{LS}) is determined by

$$V_S = \begin{cases} \sqrt{2}v \sin \omega T, 0 < T < \alpha t_S \\ V_S - V_{CS} - V_{L,} \alpha t_S < T < t_S \end{cases} \qquad (3)$$

The activity cycles of the switch S_A and S_B, the voltage over the capacitance C_S and C_L, accordingly, and V_{CS} and V_{CL}. The voltage between the capacitance C_S and C_L are inherently balanced and proportional to the output voltages, V_L, because of the SC functioning of C_S. To do this, further voltage control for C_S It is not required.

From this, we can calculate the currents via S_A, S_B, C_S, and C_L during the shifting time t_S, as well as through devices D_A–D_D, D_E, and D_F.

$$I_S = \begin{cases} I_S, 0 < T < \alpha t_S \\ 0, \alpha t_S < T < t_S \end{cases} \qquad (4)$$

$$I_{SB} = \begin{cases} \frac{I_S(\alpha-1)}{\alpha}, 0 < T < \alpha t_S \\ 0, \alpha t_S < T < t_S \end{cases} \quad (5)$$

$$I_{CS} = \begin{cases} \frac{I_S(\alpha-1)}{\alpha}, 0 < T < \alpha t_S \\ I_S, \alpha t_S < T < t_S \end{cases} \quad (6)$$

$$I_{CL} = \begin{cases} \frac{I_S(\alpha-1)(2\alpha-1)}{\alpha}, 0 < T < \alpha t_S \\ I_S(2\alpha-1), \alpha t_S < T < t_S \end{cases} \quad (7)$$

$$I_{DA}, I_{DB}, I_{DC}, I_{DD}, I_{DE} = \begin{cases} 0, 0 < T < \alpha t_S \\ I_S, \alpha t_S < T < t_S \end{cases} \quad (8)$$

$$I_{DF} = \begin{cases} \frac{I_S(\alpha-1)}{\alpha}, 0 < T < \alpha t_S \\ 0, \alpha t_S < T < t_S \end{cases} \quad (9)$$

The volt-second balancing principle states that in a stable state, the mean value of the inductance over a cycle is 0.

Therefore, you can now get the work cycles α by

$$\alpha = 1 - \frac{V}{\sqrt{2}V_L}|\sin \omega T| = 1 - M_E|\sin \omega T| \quad (10)$$

inside the range whereby $M_E = \sqrt{V}/2V_L$. A voltage at least half the incoming voltage's maximum should be present at the converter's outputs.

With a constant value twice that of a standard single-phase PFC boosting rectification in CCM, the suggested conversion is represented as

$$G = \frac{V_L}{|V_S|} = \frac{1}{2(1-\alpha)} \quad (11)$$

It is necessary to measure the semiconductor's current and capacitance under various working conditions to determine the current stress. When t_S Is the switch duration, the associated RMS present numbers are

$$I_{CS,RMS} = \sqrt{2}i\sqrt{\frac{1-\alpha}{\alpha}} \quad (12)$$

$$I_{CL,RMS} = \sqrt{2}i\sqrt{\frac{(1-\alpha)(2\alpha-1)^2}{\alpha}} \quad (13)$$

$$I_{SRMS} = \frac{V}{2\sqrt{2}R_{Load}}\sqrt{\frac{1}{(\alpha-1)^4}} \quad (14)$$

$$I_{SA,RMS}, I_{DB,RMS} = \frac{V}{2\sqrt{2}R_{Load}}\sqrt{\frac{1}{\alpha(\alpha-1)^2}} \quad (15)$$

$$I_{DA,RMS} = \frac{V}{2\sqrt{2}R_{Load}}\sqrt{\frac{1}{(1-\alpha)^3}} \quad (16)$$

It is therefore feasible to calculate the inductance values in the case when the incoming voltage is at its highest and the rippling is at

$$L = \frac{V}{2\sqrt{2}M_E F_{SA}\Delta I_L} \quad (17)$$

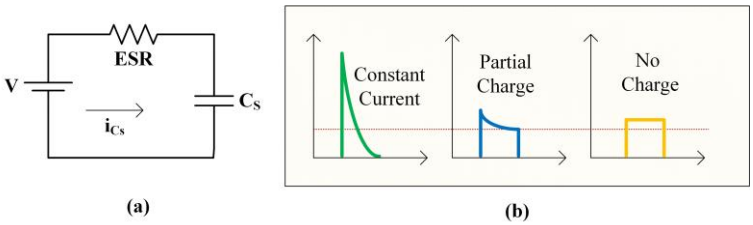


Figure 4. (a) Equivalent circuit of SC charging system. (b) Operating modes and corresponding current profiles: constant current (CC), partial charge, and no charge (NC)

ΔI_L Represents the inductance present ripples, V stands for the incoming rms voltages, and F_S Denotes the shifting frequencies. Another way to represent the DC-link capacitors, C_L, is

$$C_L = \frac{P_L}{2\pi F_S v_L \Delta v_L} \tag{18}$$

The resultant power, fluctuation of the resultant voltages, and supplying frequencies are denoted as P_L, Δv_L, and fs, correspondingly. The comparable impedance is calculated by adding the inherent resistance of the PCB track, S_A, S_B, C_S, C_L, and D_F In fig 4.

The switched-capacitance C_S The equivalent series resistance (ESR) indicates the operating state of the conversion, as shown in Figure 4(a). A temporal variable associated with the shifting time t_S It is obtained by multiplying these two quantities.

A flow $I_{CS,X}$(t) will start flowing once the capacitors begin to recharge. The link between the length τ and the temporal variable ESR*C_S Determines which of the three forms currently may take, as seen in Figure 4(b). This scenario is called complete charge (CC), and the recharging will be finished inside τ for $\tau >> ESR * C_S$, as shown in Figure 4(b). See Figure 4(b) for the fractional charges for τ ≈ ESR*Csw. As shown in Figure 4(b), the flow will remain almost steady and there will be no charges (NC) for $\tau << ESR * C_S$. Throughout the range of τ, the voltages on the capacitance will remain reasonably steady in this case. With even more stability, the output's power I_0 is equal to the mean present throughout the t_X time, $I_{CS,X}$ (the mean amount throughout a shifting phase "t_S").

$$I_{CS,X} = \frac{1}{t_S}\int_0^{t_S} I_X(T)dT = I_0 \tag{19}$$

The voltage across the capacitance throughout the t_X The Phase is denoted by I_X (t), and t_S is equal to $1/F_S$.

Advanced Control Architectures with Comprehensive System Modeling

A continuous-time reaction is produced because the averaging large-signal theory does not take into account the high-frequency fluctuations that come from the semiconductor switching. The steady-state hypothesis is applied to the inductance present (I_L) and capacitors voltages (V_{CL}When the switching is in the ON and OFF stages, the goal is to achieve this. Given that the capacitor values given are equivalent to one another (C_L = C_S = C), we can use the following phase formulas to obtain the values of I_L and V_L:

$$L\frac{dI_L}{dt} = V_S - 2(1-\alpha)V_L \tag{20}$$

$$C(1+\alpha)\frac{dV_L}{dt} = (1-\alpha)I_L - \frac{V_L}{R_{Load}} \tag{21}$$

At the selected operating point, there are steady numbers for every parameter (i_l, v_S, v_L, and α) and small-signal ac (I_l, $\widehat{v_S}$, $\widehat{v_L}$, and $\hat{\alpha}$) with tiny variations. presently,

$$I_l = i_l + \hat{I_l},\ v_S = V_S + \widehat{v_S}, v_L = V_L + \widehat{v_L}, and\ \alpha = \bar{\alpha} + \hat{\alpha} \tag{22}$$

Presently, for both (20) and (21), the representations mentioned before may be obtained in the following way:

$$L\frac{d(i_l+\widehat{I_l})}{dt} = (v_S + \widehat{v_S}) - 2(1-\bar{\alpha}-\hat{\alpha}).(V_L + \widehat{V_L}) \quad (23)$$

$$C(1+\bar{\alpha}+\hat{\alpha})\frac{d(V_L+\widehat{V_L})}{dt} = (1-\bar{\alpha}-\hat{\alpha})\left(i_l + \widehat{I_l}\right) - \frac{(V_L+\widehat{V_L})}{R_{Load}} \quad (24)$$

Rewriting equations (23) and (24) as (25) and (26) is necessary because adding two tiny ac values produces an additional small signal; therefore, the results of small ac impulses are disregarded.

$$L\frac{d\widehat{I_l}}{dt} = \widehat{v_S} - 2(1-\bar{\alpha})\widehat{v_L} + 2v_L\hat{\alpha} \quad (25)$$

$$C(1+\bar{\alpha})\frac{d\widehat{V_L}}{dt} = (1-\bar{\alpha})\widehat{I_l} - i_l\hat{\alpha} - \frac{\widehat{v_L}}{R_{Load}} \quad (26)$$

By using the Laplace transformation on equations (25) and (26), we get

$$SL\widehat{I_l}(S) = \widehat{v_S}(S) - 2(1-\bar{\alpha})\widehat{V_L}(S) + 2V_L\hat{\alpha}(S) \quad (27)$$

$$\left(SC(1+\bar{\alpha}) + \frac{1}{R_{Load}}\right)\widehat{V_L}(S) = (1-\bar{\alpha})\widehat{I_L}(S) - i_L\hat{\alpha}(S) \quad (28)$$

$$\begin{bmatrix} sl & 2(1-\bar{\alpha}) \\ (1-\bar{\alpha}) & -\left(sC(1+\bar{\alpha}) + \frac{1}{R_{Load}}\right) \end{bmatrix}\begin{bmatrix} \widehat{I_l}(S) \\ \widehat{V_L}(S) \end{bmatrix} = \begin{bmatrix} 2V_L \\ i_l \end{bmatrix}\hat{\alpha}(S) + \begin{bmatrix} 1 \\ 0 \end{bmatrix}\widehat{v_S}(S) \quad (29)$$

The current procedure involves transferring functional $G_{I\alpha}(S)$ as

$$G_{I\alpha}(S) = \frac{\widehat{I_l}(S)}{\widehat{\alpha}(S)} = \frac{\widehat{I_S}(S)}{\widehat{\alpha}(S)} = \frac{sC(1+\bar{\alpha})v_L + 6(1-\bar{\alpha})I_l}{s^2LC(1+\bar{\alpha}) + 2(1-\bar{\alpha})^2 + \frac{sL}{R_{Load}}} \quad (30)$$

Using high-frequency estimation, the transfer functions can be further reduced and shown in Fig. 5. This simplifies the transference functional in (30) by replacing the capacitance with a short circuit at higher rates, as seen below:

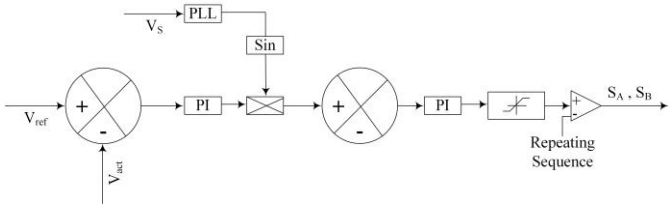


Figure 5. Closed-loop control architecture for the projected converters

$$G_{IA}(S) \approx \frac{2V_L}{sL} \quad (31)$$

It is now possible to describe the transference function for the incoming voltage. I_S/I_l and M_A:

$$\frac{\widehat{I_l}(S)}{\widehat{M_A}(S)} = \frac{\widehat{I_S}(S)}{\widehat{M_A}(S)} \approx \frac{1}{V_c} * \frac{2V_L}{sL} \approx \frac{2V_L}{sV_cL} \quad (32)$$

When the carrier's signal's highest point is V_c. In a similar vein,

$$\frac{\widehat{V_L}(s)}{\widehat{\alpha}(S)} = \left[\frac{2V_L(1-\bar{\alpha}) - sLi_L}{\frac{LC(1+\bar{\alpha})}{(1-\bar{\alpha})^2}S^2 + \frac{L}{R_L(1-\bar{\alpha})^2}S + 2}\right] \quad (33)$$

Figure 5 shows the suggested conversion with a reduced controller block architecture. Here is an example of a combined management system that can better track both AC and DC references. This is achieved by merging the voltages outside the loops with the voltages inside the present loops. Proportional-integral (PI) control enables the voltage loops to maintain stable DC output voltages.

It is crucial to maintain stable voltage regulators to minimise flow standard deviation. Harmony may be amplified by insufficient present tracking, leading to a fast reduction in the energy ratio. A significant maximum-power surge may result from improper handling, compromising the DC-link capacitor's ability to maintain balance and, in extreme cases, damaging the device [26].

The dynamic of the present regulator should be quicker than that of the voltage regulator to reduce the present inaccuracy. The incoming voltages are used to generate a symmetrical flow wave in these control loops.

The unanticipated efficiency reduction that occurs with the deployment of digitally controlled loops is due to the introduction of transportation delay, which is absent in the conventional method [27].

But this problem is reduced when this lag is accounted for in an analogue architecture. There are lags during digital implementations caused by PWM, manufacturing, and samples. Therefore, a first-order projected total delayed Noetherian pade

$$G_D(S) = \frac{1-\frac{t_D S}{2}}{1+\frac{t_D S}{2}} \tag{34}$$

that is, when t_D Is equal to TPWM. The present transfer function of the structure, the open-loop gains with transportation delay, and the PI controller's transfer function are all included in the following formula.

$$G_{I,O.L}(S) = G_{I\alpha}(S) * G_{PI}(S) * G_D(S) = \frac{2V_L}{2L} * \left(K_{p,I}\frac{K_{i,I}}{S}\right) * \left(\frac{1-\frac{t_D S}{2}}{1+\frac{t_D S}{2}}\right) \tag{35}$$

The efficiency of the present management loop is defined by the phase margin (PM) and the cross-over frequencies (ϋc). Optimising the crossover frequencies is essential to improving the conversion's THD. By utilising the frequency response of the plant's transfer function at a specific bandwidth (he ptimm cap K sub, p, cap I. end subscript and cap K sub, i., cap I. end subscript may be calculated using the SISO tool in M vaiabls $K_{p,I}$ and $K_{i,I}$ have been set to 1.13 and 0.3, respectively, for this conversion. The 60◦ PM and 8.33 kHz crossing frequencies are used to determine these numbers.

Capacitance C_S It does not affect low-frequency performance because it does not filter out low-frequency harmonics. Very high C_S Values would have a disproportionate impact on low-frequency actions. We next describe the corresponding energy of the ac output cycles as

$$P_S = P_l + P_{CL} + P_{CS} + P_{RLoad} \tag{36}$$

Where, $P_l = \frac{1}{2}L\frac{dI_S^2}{dt}, P_S = \frac{1}{2}V_{S,pK}^2, K_S, P_{CS} = \frac{1}{2}C_S\frac{dV_L^2}{dt}, P_{CL} = \frac{1}{2}C_L\frac{dV_L^2}{dt}, and\ P_{RLoad} = \frac{V_L^2}{R_{Load}}$

$$(C_S + C_L)\frac{dV_{Load}}{dt} = \frac{P_L}{V_L} * K_S - \frac{V_L}{R_{Load}} \tag{37}$$

The immediate amount of K_S The voltage adjuster adjusts the converter's output voltages. By averaging numbers, intake flow is controlled in relation to a standard input rather than the output's value. By streamlining steady-state simulation, ignoring cyclical impacts and voltage ripples, and removing constants and higher-order components from equation (40), we may get the resulting transformed transference operator:

$$V_L \frac{d\widehat{V_L}}{dt} = \frac{P_L}{(C_S+C_L)} * \widehat{K_S} - \frac{2V_L}{(C_S+C_L)R_{Load}} * \widehat{V_L} \quad (38)$$

Table 2. MATLAB simulation specifications for 850w setup

Parameter	Specification
Power Rating	850 W
Switches).	SiC MOSFET, 1400 V, r_{ds} (on) 50 mΩ
Switches (S_B)	SiC MOSFET, 750 V, r_{ds} 75 mΩ
Diodes (D_A–D_D)	SiC Diode, 1400 V, 20 A
Diodes (D_E, D_X)	SiC Diode, 1400 V, 30 A
Inductor (L_S)	1.8 mH
Capacitors (C)	470 µF × 2, 200 V DC
Switching Frequency	50 kHz

Energy electronics conversions often utilise the PIM control technique, which integrates a proportional (P) and an integrator (I) element to effectively control the output. While the integrated part keeps track of errors over time and the derivative part predicts how errors will fluctuate, the proportional part uses the error to adjust the control output. To improve the converter's efficiency and ensure precision and dependability, it is necessary to optimise the PI values (k_p = 1.3, k_i = 0.3). Applying PIM to OSBPFC conversions enables accurate power factor correction (PFC), which optimises energy use by continuously reacting to changes in supply voltages and present conditions. A more effective conversion is the result of the controller's results, which is a function of the total of the two inputs (P, I). This result guarantees effective functioning, lowers latent might, and increases energy ratio. Increased energy efficiency, lower energy expenses, and greater system effectiveness are the outcomes of selecting optimal PI increases using techniques such as Ziegler-Nichols or optimisation, as shown in Table 2.

Analytical Study of OSBPFC Converter Dynamics Via Simulation

The groundbreaking PIM included in the OSBPFC conversions is demonstrated in this lesson, along with its superior effectiveness when compared to traditional converter-controller setups. To start, we look at the converter's steady-state efficiency, which is shown in Figure 6(a) by the features of the input volts (V_S) and electricity (I_S). Its ability to efficiently extract energy while maintaining superior performance is demonstrated by the converters' outstanding PF of 0.9996. The similar numbers also show that the THDs are relatively lower at 1.17%. The variety of Fast Fourier Transforms (FFTs), as illustrated in Figure 6(b), is an extra area of performance exploration. The continuous THD of 1.17% demonstrates the planned PI approaches' capability to reduce THD relative to alternatives. The capability of the conversions to deliver consistent, clean power production is shown by these, which improves the reliability of the systems [28].

Simulation Assumptions

The MATLAB/Simulink simulation model assumes ideal component properties for lossless inductors and capacitors, with parasitic effects negligible. The converter operates at a constant switching frequency (50 kHz) in Continuous Conduction Mode (CCM) [9]. All capacitors are sized to maintain voltage stability, and input voltage variations are modelled as sinusoidal sources at 230 V RMS. They include temperature changes and non-idealities to concentrate on the assessment of the control system performance. These hypotheses allow making regular comparative analysis with the known PFC topologies under the same test conditions.

Figure 6(a) and (b) show the outcomes of evaluating the converter's dynamic performance in response to fluctuations in demand energy. It is suitable for real-world applications with rapidly varying demand, as it responds to and recovers steadily even during load fluctuations. The results demonstrate that the PIM in OSBPFC conversions is an efficient option for energy converters [29]. An extensive examination of the PIM's efficacy metrics, with an emphasis on settlement periods, rising times, and peak exceeds, yields extraordinary consequences. The increase period was less than 0.01 seconds, and the highest value exceeded 1.31%, while the setting duration was an impressive 0.092 minutes. Table 3 provides a summary of these requirements for easy examinations, and they clearly exceed those of the traditional controller’s approach.

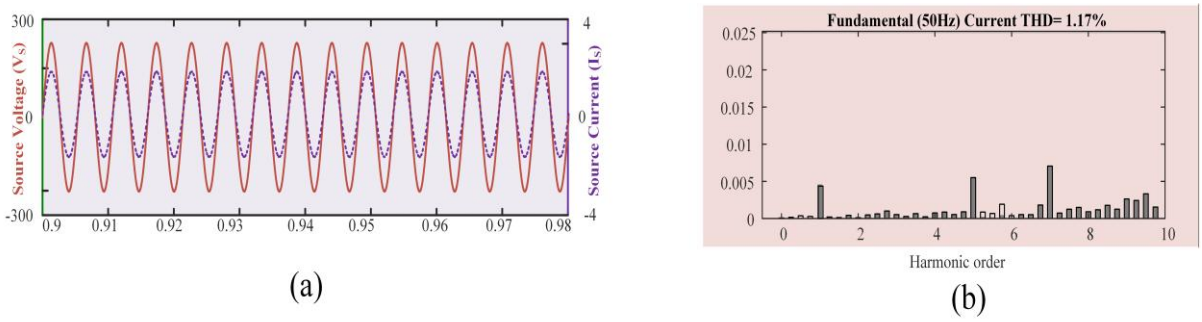


Figure 6. Simulation results illustrating the performance of the optimised converters operating with PIM control at V_S = 230V. (a) Representations of steady-state wave shapes detected at the source terminals (b) Harmonic spectrum investigation highlights the THDs

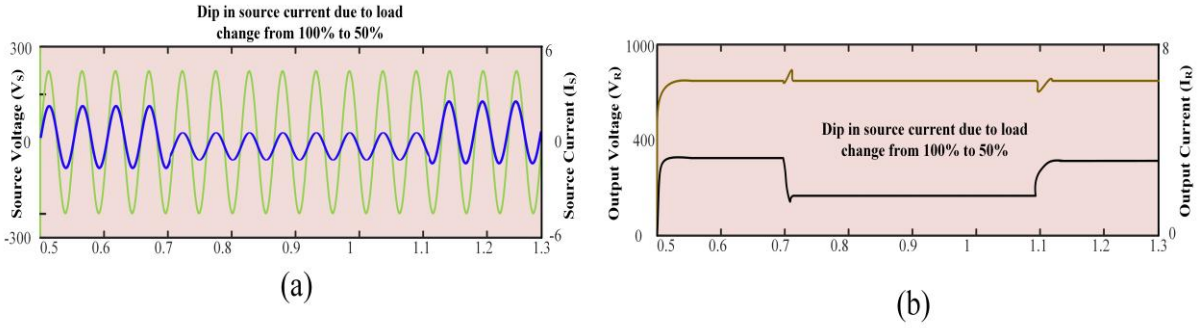


Figure 7. Simulink outcomes of optimal conversions with pim control at supply voltages V_S = 230v(a) output voltage (V_L) and output current (I_L) under 50% load condition (b) Input voltage (V_S) and input current (I_S) under 50% load condition

Also, under a standard 230 V load, we tested the effect of varying load energy on the efficiency metrics of PQ, output, and intake. Figure 7(b) presents a graphical representation of the information, providing valuable insight into control performance under a variety of loading conditions. The simulation results confirm beyond any reasonable doubt that the ideal PIM is more stable and consistent across a broad range of energy supply conditions. With a high responsiveness rate and excellent concert capabilities, the suggested controller is one of the best options for efficient PFC operations.

Table 4 presents the results of the research on workload oscillation at the Wide Loops setup. This table provides vital information on load cycle variations under different conditions, which helps understand the behaviour of the systems. It shifts attention to exploring the variations in source voltages when the Close Loops research begins.

Table 5 also showed that the setting position energies were variable relative to the closed-loop investigations. These variations show how much the proposed controllers can bring the set position values to the required level. The results presented in the table form a reasonable demonstration of performance of the suggested controller tracks in defining position energies under different conditions. To stabilise the situation and identify the most significant load variations, the critical information is presented in a table, showing the system's response to the load variations and allowing a comprehensive evaluation of the controller's performance [30]. Finally, the findings provide a detailed review of the different system characteristics and the role of the proposed controls in these works. The value of perceptions and their contribution to understanding system dynamics is highly beneficial for developing and revising control plans for related issues. Table 5 will allow analysis of the strength loss in the different parts of the converter system. Converter power losses are a significant factor in determining how effectively and thermally a device would operate. These losses may be ascribed to the different internal resources of the converter all of which serve to produce the entire loss of strength. The classification and identification of the numerical value of such losses will help in the design, enabling awareness of areas that can be optimised and developed.

In addition to its high steady-state fulfilment, controls are regularly proposed to ensure they can maintain a version in AC primary voltages, which is critical to dynamical performance. Regarding the daily setups, the counselled mixes show better performance and efficiency, as indicated in Table 6. To address variations in electrical conditions and other recognised effects in the spaces, the highlights of those records can be used to demonstrate the efficiency and usability of the proposed controllers.

Table 3. Duty ratio fluctuations in the open-loop systems

Duty Ratio	V_S (V)	I_S (A)	V_L (V)	I_L (A)	THD (%)	PF	Efficiency ($\boldsymbol{\eta}$) (%)
0.25	230.1	3.69	920.4	0.82	16.12	0.8817	88.5
0.5	234	3.63	936.8	0.78	22	0.8502	86
0.75	237	3.59	948.6	0.77	24.5	0.8201	85.8
0.8	240	3.54	966	0.74	26.2	0.7855	84.5

Table 4. Closed-loop system performance assessment under reference voltage variations

Reference Voltage (V)	**Source Voltage (V)**	**Source Current (A)**	**Load Voltage (V)**	**Load Current (A)**	**Power Factor**	**Source Harmonics (%)**	**Efficiency (%)**
840	230	3.69	842	0.95	0.9994	1.29	93.9
880	230	3.69	888	0.91	0.9996	1.24	95.2
920	230	3.69	920	0.89	0.9997	1.17	97.00
960	230	3.69	966	0.85	0.9996	1.24	96.40
1000	230	3.69	1005	0.81	0.9996	1.25	95.98

Table 5. Breakdown of power losses in converter components

Component	**Description of Loss**	**Magnitude (W)**
MOSFET Conduction Loss	Power is dissipated by the current flowing through the MOSFET's internal resistance during operation.	1.72
MOSFET Switching Loss	Losses during MOSFET switching transitions are influenced by switching frequency and gate charge.	2.2
Diode Conduction Loss	Energy is lost as heat when current flows through the diode during conduction.	7.658
Diode Switching Loss	Power loss occurs during the diode's transition phases, depending on recovery time and current levels.	1.75
Inductor Loss	Losses are attributed to the resistance in the inductor winding, proportional to the square of the current.	8.2
Capacitor Loss	Energy is dissipated in capacitors due to their equivalent series resistance, regardless of whether the current is AC or DC.	1.22
Miscellaneous Loss	Includes all other minor losses not specifically categorised under the listed components.	2.89
Total Losses	The sum of all power losses from the converter components.	25.64

Table 6 provides a simple yet informative comparison of the proposed converter and available designs with respect to critical parameters and performance measures. The assessment is expected to show the improvements of the proposed methodology that are not related to its irrelevance to industry standards. Efficiency, power density, cost-effectiveness, complexity, and operational reliability are the critical elements compared to others. The analysis takes into account a variety of past research designs, overall enterprise implementation, and prototypes developed in the literature. These later designs form the foundation of the effectiveness of the suggested converter.

Table 6. Simplified comparison of the proposed converter with existing designs

Converter	Key Components	Sensors	Mode	Input Range (V)	Output (V)	Efficiency (%)	Drivers	Voltage/Current Stress
[2]	L: 4, S: 2, D: 4, C: 4 (14)	3 (2V, 1I)	CCM	220	380	95.8 @ 0.4 kW	4	Low
[4]	L: 8, S: 2, D: 5, C: 4 (19)	1 (V)	DCM	220	48	93.4 @ 0.1 kW	3	Moderate
[14]	L: 7, S: 2, D: 8, C: 7 (24)	1 (V)	CCM	180-260	52	93.75 @ 0.114 kW	2	High
[15]	L: 5, S: 10, D: 0, C: 2 (17)	1 (V)	CCM	220	500	95.5 @ 3.6 kW	2	Moderate
[12]	L: 3, S: 1, D: 4, C: 5 (14)	3 (2V, 1I)	CCM	85-265	200-400	95.3 @ 1.0 kW	2	Low
Proposed	L: 1, S: 2, D: 6, C: 2 (12)	3 (2V, 1I)	CCM	230	920	97 @ 0.85 kW	2	Moderate

Practical Implications

The refined OSBPFC converter demonstrates tangible advantages in AC-DC implementations for industrial and consumer-grade applications. It better aligns with high-density power supplies, EV chargers, and renewable energy interfaces due to its excellent dynamic behaviour and 97% efficiency. The extremely small THD (1.17) and the power factor close to unity indicates that the standard of harmonic control 61000-3-2 specified by the IEC standard is satisfied. Also, it is designed as a single-stage converter, resulting in minimal heat loss and reduced stress on its components, thereby extending converter life and reducing maintenance. These findings support the claim that the proposed converter is superior not only in theory but also in practice for energy systems that require a high degree of reliability and power quality.

CONCLUSION

Ultimately, the study proposes a special One-Stage Boosting Power Factor Correction (OSBPFC) converter with an advanced control method that complements its internal laws, balance, and robustness. The suggested strategy is seen as a contrast to conventional techniques in that it offers outstanding overall performance —i.e., short upward push times and low overshoot —and alleviates the shortcomings of traditional AC-DC converters. The advanced general performance of the converter, in terms of its robustness to load changes and voltage disturbances, is determined through rigorous evaluation involving MATLAB/Simulink modelling and simulation with the current answers. Although the strength was closer to solid-state, with a Total Harmonic Distortion (THD) of 1.17, the device was called the one that mind-blows operational efficiency (97%) and has a powerful brief conduct. This is an excellent advancement in energy conversion generation. It lays the groundwork for more sophisticated controllers that ensure accurate regulation and superior electricity quality across a broad spectrum of applications. Besides validating the simulation, the converter architecture offered may also be extended to electric vehicle charging systems, renewable energy converters, and aerospace power modules that require small, high-efficiency AC-DC interfaces. It can also be used in smart grid and data centre power supply applications due to its low THD and high efficiency. The scalability of the converters for industrial use can be further studied by implementing digital control on DSP- or FPGA-based platforms and testing them under non-ideal component conditions in the future.

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